WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate; and

a non-volatile memory cell provided on the semiconductor substrate,

the non-volatile memory cell comprising:

a tunnel insulating film having a film thickness periodically and continuously changing in a channel width direction of the non-volatile memory cell;

a floating gate electrode provided on the tunnel insulating film;

a control gate electrode provided above the floating gate electrode; and

an interelectrode insulating film provided between the control gate electrode and the floating gate electrode.

2. The semiconductor device according to claim 1,

wherein a height of an interface between the tunnel insulating film and the semiconductor substrate periodically and continuously changes in the channel width direction.

3. The semiconductor device according to claim 2,

wherein an upper surface of the tunnel insulating film is nearly flat.

4. A semiconductor device comprising:

a semiconductor substrate; and

a non-volatile memory cell provided on the

semiconductor substrate,

the non-volatile memory cell comprising:

a tunnel insulating film having an approximately constant film thickness, a height of an interface between the tunnel insulating film and the semiconductor substrate periodically and continuously changing in a channel width direction of the non-volatile memory cell;

a floating gate electrode provided on the tunnel insulating film, a height of an interface between the floating gate electrode and the tunnel insulating film periodically and continuously changing in the channel width direction of the non-volatile memory cell;

a control gate electrode above the floating gate electrode; and

an interelectrode insulating film provided between the control gate electrode and the floating gate electrode.

5. A method of manufacturing a semiconductor device comprising: a semiconductor substrate; an isolation region provided on a surface of the semiconductor substrate and including an isolation trench; and a non-volatile memory cell provided on the semiconductor substrate, the non-volatile memory cell comprising: a tunnel insulating film; a floating gate electrode provided on the tunnel insulating film; a control gate electrode above the floating gate

electrode; and an interelectrode insulating film provided between the control gate electrode and the floating gate electrode,

the method comprising:

forming an insulating film to be processed into the tunnel insulating film on the semiconductor substrate;

forming a semiconductor film to be processed into the floating gate electrode on the insulating film;

forming the isolation trench by etching the semiconductor film, the insulating film and the semiconductor substrate; and

annealing the floating gate electrode, the tunnel insulating film and the semiconductor substrate in water vapor atmosphere.

6. The method of manufacturing the semiconductor device according to claim 5,

wherein the tunnel insulating film includes a portion whose thickness increases gradually toward the isolation region.

7. The method of manufacturing the semiconductor device according to claim 6,

wherein the portion whose thickness increases gradually toward the isolation region exists in a channel width direction section of the non-volatile memory cell.

8. The method of manufacturing the semiconductor

device according to claim 6,

wherein an upper surface of the isolation region is higher than the surface of the semiconductor substrate, and lower than an upper surface of the floating gate electrode, and

the tunnel insulating film includes a first portion and a second portion in the channel width direction section of the non-volatile memory cell after the annealing the floating gate electrode, the tunnel insulating film and the semiconductor substrate in the water vapor atmosphere, the first portion being gotten into between the lower side of the floating gate electrode and the isolation region, the second portion being gotten into between the upper side of a semiconductor region of the semiconductor substrate defined by the isolation region and the isolation region.

9. The method of manufacturing the semiconductor device according to claim 7,

wherein an upper surface of the isolation region is higher than the surface of the semiconductor substrate, and lower than an upper surface of the floating gate electrode, and

the tunnel insulating film includes a first portion and a second portion in the channel width direction section of the non-volatile memory cell after the annealing the floating gate electrode, the tunnel insulating film and the semiconductor substrate in the

water vapor atmosphere, the first portion being gotten into between the lower side of the floating gate electrode and the isolation region, the second portion being gotten into between the upper side of a semiconductor region of the semiconductor substrate defined by the isolation region and the isolation region.

10. The method of manufacturing the semiconductor device according to claim 5,

wherein the water vapor atmosphere includes heavy water vapor.

11. The method of manufacturing the semiconductor device according to claim 6,

wherein the water vapor atmosphere includes heavy water vapor.

12. The method of manufacturing the semiconductor device according to claim 8,

wherein the first portion of the tunnel insulating film has a dimension becoming gradually larger toward a downward direction in the channel width direction,

the floating gate electrode contacting with the first portion of the tunnel insulating film has a dimension becoming gradually smaller toward the downward direction in the channel width direction,

the second portion of the tunnel insulating film has a dimension becoming gradually larger toward an upward direction in the channel width direction, and

the semiconductor region contacting with the

second portion of the tunnel insulating film has a dimension becoming gradually smaller toward a downward direction of the semiconductor region in the channel width direction.

13. The method of manufacturing the semiconductor device according to claim 9,

wherein the first portion of the tunnel insulating film has a dimension becoming gradually larger toward a downward direction in the channel width direction,

the floating gate electrode contacting with the first portion of the tunnel insulating film has a dimension becoming gradually smaller toward the downward direction in the channel width direction,

the second portion of the tunnel insulating film has a dimension becoming gradually larger toward an upward direction in the channel width direction, and

the semiconductor region contacting with the second portion of the tunnel insulating film has a dimension becoming gradually smaller toward a downward direction of the semiconductor region in the channel width direction.

14. The method of manufacturing the semiconductor device according to claim 5,

wherein the annealing the floating gate electrode, the tunnel insulating film and the semiconductor substrate includes a first heat treatment which is carried out under a condition that water diffusion rate

in the tunnel insulating film is larger than oxidative reaction rate of the water with the floating gate electrode and oxidative reaction rate of the water with the semiconductor substrate.

15. The method of manufacturing the semiconductor device according to claim 6,

wherein the annealing the floating gate electrode, the tunnel insulating film and the semiconductor substrate includes a first heat treatment which is carried out under a condition that water diffusion rate in the tunnel insulating film is larger than oxidative reaction rate of the water with the floating gate electrode and oxidative reaction rate of the water with the semiconductor substrate.

16. The method of manufacturing the semiconductor device according to claim 14,

wherein the tunnel insulating film comprises silicon oxide or silicon oxynitride, the floating gate electrode comprises polysilicon, the semiconductor substrate comprises silicon, and the first heat treatment is carried out at temperature of 750°C or less.

17. The method of manufacturing the semiconductor device according to claim 14,

wherein the annealing the floating gate electrode, the tunnel insulating film and the semiconductor substrate includes a second heat treatment which is

carried out under a condition that water diffusion rate in the tunnel insulating film is smaller than oxidative reaction rate of the water with the floating gate electrode and oxidative reaction rate of the water with the semiconductor substrate.

18. The method of manufacturing the semiconductor device according to claim 17,

wherein the tunnel insulating film comprises silicon oxide or silicon nitride, the floating gate electrode comprises polysilicon, the semiconductor substrate comprises silicon, and the second heat treatment is carried out at temperature of 900°C or more.

19. The method of manufacturing the semiconductor device according to claim 5,

wherein the floating gate electrode has an upper surface and a side surface, the only upper surface between the surfaces is essentially covered with the interelectrode insulating film, the process of forming the interelectrode insulating film includes a first radical nitration process.

20. The method of manufacturing the semiconductor device according to claim 19,

wherein forming the interelectrode insulating film includes a silicon nitride deposition process carried out after the first radical nitriding process and a second radical nitriding process carried out after the

silicon nitride deposition process.